



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/723,451	11/28/2000	Timothy W. Fuehrer	3-48-26-2	6804

7590 02/26/2004

Docket Administrator
Agere Systems Inc.
P. O. Box 614
Berkeley Heights, NJ 07922-0614

EXAMINER

PHAM, TUAN

ART UNIT PAPER NUMBER

2643

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/723,451

Applicant(s)

FUEHRER ET AL.

Examiner

TUAN A PHAM

Art Unit

2643

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 November 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 5.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: the output differential signal pair 21 (see page 6, ln.3) in the specification is not correlated with the output differential signal pair 19 in the figure 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-6, 9-12, 14-23, 25-28, 30, and 33-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Prendergast et al. (Pub. No: U.S. 2001/0036261, hereinafter, "Prendergast").

Regarding claims 1, 21, and 30, Prendergast teaches an electrical interface (see figure 3), comprising:

a primary inductor and a secondary inductor for operable coupling an input differential signal pair to an output differential signal pair (see figure 3, isolation transformer 110, page 10, [0135] to [0138]), and

a filter that attenuates a signal occurring in the output differential signal pair (see figure 3, digital filter 108, [0135] to [0138]).

Regarding claims 2, 22, and 33, Prendergast further teaches the interface wherein the filter acts as a low pass filter and wherein the electrical interface further includes a high-pass filter, the low-pass filter and the high-pass filter having overlapping cut-off frequencies (see page 1, [0010]).

Regarding claims 3 and 34, Prendergast further teaches the interface wherein the low-pass filter and the high-pass filter together attenuate signals over a frequency range of approximately 50 kHz to approximately 10 MHz (see page 1, [0008]). It is inherently that the interface is disclosed in Prendergast's reference supporting the high-speed transmission such as HDSL2 and VDSL. Therefore, the interface should be support over 10MHz frequency range.

Regarding claim 4, Prendergast further teaches the interface wherein the primary inductor is connected between two signal paths forming the input differential signal pair (see figure 3, page 1, [0010] to [0011]).

Regarding claims 5 and 23, Prendergast further teaches the interface wherein the primary inductor forms the primary winding of a transformer (see figure 3, transformer 110).

Regarding claims 6 and 35, Prendergast further teaches the interface wherein the secondary inductor is connected between two signal paths forming the output differential signal pair and wherein the secondary inductor forms the secondary winding of the transformer (see figure 3, transformer 110, page 1, [0010] to [0011]).

Regarding claims 9 and 25, Prendergast further teaches the interface wherein the filter includes an output attenuation element for operable coupling a signal path of the output differential signal pair to ground (see page 1, [0011]).

Regarding claims 10 and 26, Prendergast further teaches the interface wherein the output attenuation element includes a resistor and a capacitor connected in parallel (see figure 3, digital filter 108). It is inherently that the digital filter should be including a resistor and a capacitor.

Regarding claims 11 and 27, Prendergast further teaches the interface wherein the output attenuation element forms a low-pass filter (see figure 3, POTS filter 116, page 2, [0014]).

Regarding claims 12 and 28, Prendergast further teaches the interface further including an input attenuation element operable coupled to at least one of the signal paths forming the input differential signal pair (see figure 3).

Regarding claim 14, Prendergast further teaches the interface wherein the input attenuation element forms a high-pass filter (see figure 3, HPF 100).

Regarding claim 15, Prendergast further teaches the interface wherein the filter attenuates a common mode signal in the output differential signal pair (see page 14, [0174] to [0178]).

Regarding claim 16, Prendergast further teaches the interface wherein the interface is adapted for being operable coupled between a codec and a digital circuit (see figure 3).

Regarding claim 17, Prendergast further teaches the interface wherein the interface further includes a codec that generates two signal paths that together form the input differential signal pair (see figure 3).

Regarding claim 18, Prendergast further teaches the interface further including an analog front end for operable coupling the codec to a telephone line (see figure 3, AFE 112, ADC 114, TIP-RING 92).

Regarding claim 19, Prendergast further teaches the interface wherein the analog front end includes circuitry for providing power to the codec from the telephone line (see figure 29, page 14, [0176]).

Regarding claim 20, Prendergast further teaches the interface wherein the analog front end includes a shunt regulator. It is inherently that the AFE should be includes a shunt regulator.

Regarding claim 36, Prendergast further teaches the method wherein the filtering step includes the step of attenuating high-frequency signals in the output differential signal pair (see figure 3, POTS filter 116, page 6, [0093]). It is inherently that the POTS filter couples to the output, which attenuate the high frequency signals.

Regarding claim 37, Prendergast further teaches the method further including the step of attenuating low-frequency signals in the input differential signal pair (see figure 3, HPF 100, page 1, [0010]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 7-8, 24, and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prendergast et al. (Pub. No. U.S.2001/0036261, hereinafter, "Prendergast") in view of Viadella et al. (U.S Patent No. 6,385,315, hereinafter, "Viadella").

Regarding claims 7, 24, and 31, Prendergast further teaches an electrical interface (see figure 3), comprising:

a primary inductor and a secondary inductor for operable coupling an input differential signal pair to an output differential signal pair (see figure 3, isolation transformer 110, page 10, [0135] to [0138]), and

a filter that attenuates a signal occurring in the output differential signal pair (see figure 3, digital filter 108, [0135] to [0138]).

It should be noticed that Prendergast fails to clearly teach a parasitic capacitor operable coupled between the primary inductor and the secondary inductor. However, Viadella teaches such features (see figure 11, capacitor 108, inductor 106) for a purpose of reducing the common mode choke signal from interfering with the devices.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of capacitor operable coupled between the primary inductor and the secondary inductor, as taught by Viadella, into view of Prendergast in order to improved the noise signal and data signal being transmitted over the telephone line.

Regarding claims 8 and 32, Prendergast further teaches the interface wherein the parasitic capacitor has a capacitance is in the range of approximately 0.5 pF to approximately 2.5 pF (see col.8, ln.55-60).

8. Claims 13 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prendergast et al. (Pub. No. U.S.2001/0036261, hereinafter, "Prendergast") in view of Holthaus et al. (U.S Patent No. 5,832,076, hereinafter, "Holthaus").

Regarding claim 13 and 29, Prendergast further teaches an electrical interface (see figure 3), comprising:

a primary inductor and a secondary inductor for operable coupling an input differential signal pair to an output differential signal pair (see figure 3, isolation transformer 110, page 10, [0135] to [0138]), and

a filter that attenuates a signal occurring in the output differential signal pair (see figure 3, digital filter 108, [0135] to [0138]).

It should be noticed that Prendergast fails to clearly teach the interface wherein the input attenuation element includes a resistor and a capacitor connected in series. However, Holthaus teaches such features (see figure 1, C1, R1) for a purpose discharging the power through the resistor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of a resistor and a capacitor connected in series, as taught by Holthaus, into view of Prendergast in order to protected the circuit that could cause failure by the high voltage.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In order to expedite the prosecution of this application, the applicants are also requested to consider the following references. Although Rahamim et al. (U.S. Patent No. 6,081,586), Embree et al. (U.S. Patent No. 6,169,762), Folwell et al. (U.S. Patent No. 5,369,666), and Chen (U.S. Patent No. 5,515,433) are not applied into this Office Action, they are also called to Applicants attention. They may be used in future Office Action(s). These references are also concerned for supporting the interface devices providing electrical isolation and resistance forward telephone line feed circuit.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tuan A. Pham** whose telephone number is (703) 305-4987 and E-mail address is: **tuan.pham@USPTO.GOV**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Curtis Kuntz, can be reached on (703) 305-4708 and

IF PAPER HAS BEEN MISSED FROM THIS OFFICIAL ACTION PACKAGE, PLEASE CALL Customer Service at (703) 306-0377 FOR THE SUBSTITUTIONS OR COPIES.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or faxed to:

(703) 872-9306

Application/Control Number: 09/723,451

Page 10

Art Unit: 2643

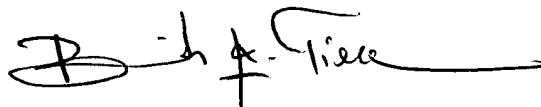
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal
Drive, Arlington VA, Sixth Floor (Receptionist, tel. No. 703-305-4700).

Art Unit 2643

Date: February 4, 2004

Examiner

Tuan Pham

A handwritten signature in black ink, appearing to read "Binh Tieu", with a long horizontal flourish extending to the right.

BINH TIEU
PRIMARY EXAMINER